

WHAT IS CLAIMED IS:

- 1 1. A voltage controlled oscillator comprising:
2 a first VCO element having an output;
3 a second VCO element having an input and an output, the input coupled to the
4 output of the first VCO element;
5 a first gated circuit having an input and an output, the input coupled to the output
6 of the first VCO element;
7 a second gated circuit having an input and an output, the input coupled to the
8 output of the second VCO element; and
9 a first logic circuit configured to receive a VCO enable signal, the output of the
10 first VCO element, and the output of the second VCO element, and further configured to provide
11 a first output enable signal to the first gated circuit and a second output enable signal to the
12 second gated circuit.
- 1 2. The voltage controlled oscillator of claim 1 wherein the first logic circuit
2 retimes the VCO enable signal with a signal at the output of the first VCO element to provide the
3 first output enable signal.
- 1 3. The voltage controlled oscillator of claim 2 wherein the first logic circuit
2 retimes the VCO enable signal using a register.
- 1 4. The voltage controlled oscillator of claim 2 wherein the first logic circuit
2 retimes the first output enable signal with a signal at the output of the second VCO element to
3 provide the second output enable signal.
- 1 5. The voltage controlled oscillator of claim 4 wherein the first logic circuit
2 retimes the first output enable signal using a register.
- 1 6. The voltage controlled oscillator of claim 5 wherein the first logic circuit
2 retimes the first output enable signal using a latch.

1 7. The voltage controlled oscillator of claim 2 wherein the output of the first
2 gated circuit couples to a first counter and the output of the second gated circuit coupled to the
3 second gated counter.

1 8. The voltage controlled oscillator of claim 2 wherein the first VCO element
2 and the second VCO element form a portion of a ring oscillator.

1 9. The voltage controlled oscillator of claim 2 wherein the output of the first
2 VCO element is buffered by a first buffer and the output of the second VCO element is buffered
3 by a second buffer.

1 10. The voltage controlled oscillator of claim 2 wherein the voltage controlled
2 oscillator is formed on an integrated circuit.

1 11. The voltage controlled oscillator of claim 10 wherein the VCO enable
2 signal is generated following an increase in a supply voltage for the integrated circuit.

1 12. The voltage controlled oscillator of claim 2 wherein the VCO enable
2 signal is a reset signal that resets a counter.

1 13. A method of enabling outputs of a voltage controlled oscillator
2 comprising:
3 receiving a VCO enable signal;
4 receiving a first VCO output signal;
5 receiving a second VCO output signal, the second VCO output signal phase
6 shifted from the first VCO output signal; and
7 retiming the VCO enable signal with the first VCO output signal to generate a
8 first VCO output enable signal.

1 14. The method of claim 13 further comprising:
2 retiming the first VCO output enable signal with the second VCO output signal to
3 generate a second VCO output enable signal.

1 15. The method of claim 13 wherein when the first VCO output enable signal
2 is asserted, the first VCO output signal is received by a logic circuit.

1 16. The method of claim 15 wherein the logic circuit is a counter.

1 17. The method of claim 15 wherein the logic circuit is a first-in-first-out
2 memory.

1 18. A voltage controlled oscillator comprising:
2 means for generating a plurality of clock outputs including a first clock output and
3 a second clock output, the first and second clock outputs shifted in phase relative to each other;
4 means for gating the first clock output and the second clock output;
5 means for receiving a VCO enable signal; and
6 means for retiming the VCO enable signal to the first clock output to generate a
7 first gating signal,
8 wherein the first gating signal controls the means for gating the first clock output.

1 19. The voltage controlled oscillator of claim 18 further comprising:
2 means for retiming the first gating signal using the second clock output to
3 generate a second gating signal,
4 wherein the second gating signal controls the means for gating the second clock
5 output.

1 20. The voltage controlled oscillator of claim 19 further comprising:
2 means for counting pulses of the gated first clock output to generate a first counter
3 output.